What is claimed is:

1. A high-speed FFT processing method comprising:

dividing a plurality of data (N) into a plurality of blocks suitable for accessing memory to be used in FFT processing;

sequentially transferring to the memory the blocks;

performing FFT processing of the FFT data in each of the block transferred to the memory; and

repeating the FFT processing until the data in all of the blocks are processed.

2. The high-speed FFT processing method according to claim 1, further comprising:

dividing the FFT processing of the plurality of FFT data into a plurality of stages; and

re-arranging the FFT data between each of the stages.

3. The high-speed FFT processing method according to claim 1, wherein the FFT data is divided such that the data falls within a range to obviate resetting of a bank constituting the memory at the time of memory access.

4. The high-speed FFT processing method according to claim 1, wherein the FFT data is divided such that the data falls within a range to obviate resetting of a row address or column address at the time of memory access.

5. The high-speed FFT processing method according to claim 1, wherein the FFT data constitutes real and imaginary parts and are subjected to FFT processing with a rotator.

6. The high-speed FFT processing method according to claim 5, wherein the rotator is preserved in a table in advance to correspond to each of the blocks.

7. The high-speed FFT processing method according to claim 5, wherein the processing of imaginary data in the FFT data is omitted.

8. The high-speed FFT processing method according to claim 5, wherein multiplication in FFT processing is omitted when the real part or imaginary part of the rotator is zero.

9. An FFT processing system comprising:

a bulk storage unit for storing a plurality of data (N);

an FFT processing unit for performing FFT processing;

a high-speed access memory accessed at the time of the FFT processing;

a dividing section for dividing the plurality of data into M blocks suitable for access to the high-speed access memory, where $M = 2^m$;

a first transfer section for transferring the blocks of the data from the bulk storage unit to the high-speed access memory; and

a second transfer section for transferring a result of FFT processed performed by the FFT processing unit to an original storage position in the bulk storage unit through the high-speed access memory and a re-arrangement processing section, on the basis of data stored in the high-speed access memory.

10. The FFT processing system according to claim 9, wherein the FFT processing unit comprises a first through n^{th} FFT processing sections; and

the first through n^{th} FFT processing sections perform FFT processing operations for first through n^{th} stages.

11. The FFT processing system according to claim 9, wherein the FFT processing unit comprises:

M number of first FFT processing sections ($M = 2^m$); and

K of second FFT processing sections ($K = 2^k$); and

the first FFT processing sections perform FFT processing operation for a first stage, and the second FFT processing sections perform FFT processing operations for a second stage.

12. The FFT processing system according to claim 11, wherein the dividing section has a re-arrangement processing

function for re-arranging the data during a period between a current stage and the next stage.

13. The FFT processing system according to claim 9, wherein the FFT data include real-part data and imaginary-part data and are to be subjected to FFT processing with a rotator.

14. The FFT processing system according to claim 13, wherein the rotator is preserved in a table in advance to correspond to each of the blocks.

15. The FFT processing system according to claim 13, wherein the processing of imaginary data in the data is omitted.

16. The FFT processing system according to claim 1, wherein, multiplication in the FFT processing is omitted when the real part or imaginary part of the rotator is zero.